A HIGH SPEED DRAM ARCHITECTURE WITH UNIFORM ACCESS LATENCY

[0001] This application is a continuation application from United States Application No. 10/336,850, filed January 6, 2003, now Patent Number 6,711,083 which is a continuation application from PCT International Application No. PCT/CA/01/00949, filed June 29, 2001, which claims priority from Canadian Application Serial No. 2,313,954, filed July 7, 2000 and United States Application No. 60/216,679, filed July 7, 2000.

[0002] The present invention relates generally to high-speed DRAM architectures, and specifically to timing of read, write and refresh operations.

BACKGROUND OF THE INVENTION

[0003] Traditionally, the design of commodity of Dynamic Random Access Memory (DRAM) devices is more focused on achieving low cost-per-bit through high aggregate bit density than on achieving higher memory performance. The reason for this is the cell capacity of a two dimensional memory array increases quadratically with scaling, while the overhead area of bit line sense amplifiers, word line drivers, and row address (or x-address) and column address (or y-address) decoders increase linearly with scaling. Therefore, the design emphasis focus on memory density has resulted in commodity DRAMs being designed having sub-arrays as large as practically possible, despite its strongly deleterious effect on the time needed to perform cell readout, bit line sensing, cell restoration and bit line equalization and precharge. As a result, the relatively low performance of traditional DRAM architectures as compared to Static Random Access Memory (SRAM) has generally limited its use to large capacity, high density, cost sensitive applications where performance is secondary.

[0004] Furthermore, traditional DRAM architectures minimize the number signal pins on memory devices by multiplexing address lines between the row and column components of the address. As a result, the two dimensional nature of DRAM array organization has always been an inherent part of the interface between memory control or logic and DRAM memory devices.

[0005] The advent of synchronous interface DRAM technologies such as SDRAM, direct RAMBUS, and double data rate (DDR) SDRAM has replaced the separate row and column